IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A magnetic random access memory comprising:

a plurality of cell units, each ~~of which comprises~~ cell unit including a plurality of cross-point memory cells ~~that~~ having first and second terminals and configured to exhibit a magnetoresistive effect;

a plurality of word lines, each ~~of which is~~ word line being connected to ~~one terminal~~ the first terminals of a corresponding ~~one~~ first pluralilty of the cross-point memory cells in each cell unit;

a plurality of sub bit lines, each ~~of which is commonly~~ sub bit line being connected to the ~~other terminal~~ second terminals of ~~each~~ a second corresponding plurality of the ~~plurality of~~ cross-point memory cells so as to form ~~a predetermined unit~~ sub bit line interconnected units in each cell unit;

a plurality of main bit lines, ~~which are commonly~~ each main bit line being connected to ~~said plurality of~~ at least one sub bit line interconnected unit in each cell unit by corresponding sub bit lines through first switch circuits [[,]] ~~respectively~~[[,]] and ~~form~~ forming a hierarchical bit line structure together with the sub bit lines in each cell unit;

a column select circuit configured to select ~~the~~ one main bit line and to connect the selected one main bit line to a sense amplifier; and

a row select circuit configured to select ~~the~~ one word line ~~for each~~ at a time from a corresponding cell unit connected to a selected cross-point memory cell by controlling ~~the switch~~ selecting circuits[[,]] ~~and in~~ during a read operation[[,]] to set[[,]] ~~in a floating state~~[[,]] all other ~~the~~ word lines ~~except~~ in the cell unit having the selected word line ~~with a selected memory cell connected~~[[,]] to a floating state while maintaining a different state for ~~which unselected memory cells connected to the sub bit line to which~~ the one selected

~~memory cell is connected are connected~~[[,]] word line and to set the word lines ~~connected to the memory cells in the cell unit which does not include the selected memory cell~~ in the cell units not having the one selected word line to ~~the~~ a same potential as that ~~of~~ normally applied to all the main bit ~~line~~ lines.

Claim 2 (Currently Amended): The memory according to claim 1, wherein the plurality of cross-point memory cells in each cell unit ~~is a memory cell block in which the memory cells~~ are laid out in a matrix[[,]] ~~one terminal of each of the memory cells in each memory cell block is connected to a corresponding one~~ with the plurality of ~~the~~ word lines in each cell unit forming each matrix ~~for each~~ row, and ~~the other terminal is connected to a corresponding one of the~~ each main bit line and connected sub bit line interconnected unit in each cell unit forming each matrix ~~lines for each~~ column.

Claim 3 (Currently Amended): The memory according to claim 1, wherein ~~the~~ each first switch circuit includes a first MOS transistor ~~which has~~ having a current path ~~whose~~ with one end ~~is~~ connected to the sub bit line of a corresponding sub bit line interconnected unit and ~~whose other~~ with an opposite end ~~is~~ connected to ~~the~~ a corresponding main bit line, ~~for each column and which~~ wherein each first MOS transistor is ON/OFF-controlled by a cell unit select signal output from the row select circuit.

Claim 4 (Currently Amended): The memory according to claim 1, wherein the column select circuit comprises:

a plurality of second MOS transistors, each second MOS transistor ~~for column selection, which has~~ having a current path ~~whose~~ with one ~~terminal is~~ end connected to ~~the~~ a

corresponding main bit line and ~~whose other terminal is~~ with an opposite end connected to the sense amplifier,

a plurality of column select lines with each column select line ~~which is~~ connected to ~~a~~ each gate of ~~the~~ each second MOS transistor,

a CSL driver ~~which outputs~~ configured to output a column address select signal to ~~the~~ a selected column select line to selectively drive the selected column select line,

a column decoder ~~which decodes~~ configured to decode a column address signal and ~~supplies~~ to supply the column address signal to the CSL driver, and

a first bias circuit ~~which~~ configured to selectively ~~applies~~ apply a bias voltage to ~~the~~ each main bit line on the basis of the column address select signal output from the CSL driver.

Claim 5 (Currently Amended): The memory according to claim 1, wherein the row select circuit includes,

a read word line driver ~~which~~ configured to selectively ~~drives~~ control the states of the word ~~line for~~ lines in each cell unit and to control ~~controls~~ the first switch circuit ~~for~~ connected between each sub bit line interconnected unit and each main bit line in each cell unit to connect the sub bit line interconnected unit in the cell unit which includes the selected cross-point memory cell to the main bit line being selected, and

a row decoder ~~which decodes~~ configured to decode a row address signal and ~~supplies~~ to supply the row address signal to the read word line driver.

Claim 6 (Currently Amended): The memory according to claim 1, wherein the ~~row select circuit includes a~~ selecting circuits include a plurality of third MOS transistors, each third MOS transistor ~~which has~~ having a current path ~~whose~~ with one end ~~is~~ connected to one

end of ~~the~~ each word line and ~~whose other~~ with an opposite end ~~is~~ commonly connected [[,]] to a second bias circuit ~~which applies~~ configured to apply a bias voltage to said ~~other terminal~~ opposite end of ~~the~~ each third MOS transistor, a first read word line driver ~~which drives the~~ configured to selectively drive each third MOS transistor for each cell unit, a first row decoder ~~which decodes~~ configured to decode a row address signal and supplies the row address signal to the first read word line driver, a plurality of fourth MOS transistors, each fourth MOS transistor ~~which has~~ having a current path ~~whose~~ with one end ~~is~~ connected to ~~the other~~ a second end of ~~the~~ each word line and ~~whose other~~ with an opposite end ~~is~~ commonly connected, a second read word line driver ~~which~~ configured to selectively ~~drives~~ ~~the~~ drive a fourth MOS transistor and ~~controls~~ to control the first switch ~~circuit~~ circuits for each cell unit to connect ~~the~~ a sub bit line interconnected unit in the cell unit which includes the selected cross-point memory cell to the corresponding main bit line, and a second row decoder which decodes the row address signal and supplies the row address signal to the second read word line driver.

Claim 7 (Currently Amended): The memory according to claim 1, wherein the ~~row select circuit includes~~ selecting circuits include a plurality of third MOS transistors, each ~~includes a~~ third MOS transistor ~~which has~~ having a current path ~~whose~~ with one end ~~is~~ connected to one end of ~~the~~ each word line and ~~whose other~~ with an opposite end ~~is~~ commonly connected[[,]] to a second bias circuit ~~which applies~~ configured to apply a bias voltage to the ~~other terminal~~ opposite end of ~~the~~ each third MOS transistor, a fourth MOS transistor ~~which has~~ having a current path ~~whose~~ with one end ~~is~~ connected to ~~the other~~ a second end of ~~the~~ each word line and ~~whose other~~ with an opposite end ~~is~~ commonly connected, a read word line driver ~~which~~ configured to selectively ~~drives the~~ drive a fourth MOS transistor and ~~controls~~ to control the first switch ~~circuit~~ circuits and the third MOS

~~transistor~~ transistors for each cell unit to connect ~~the~~ a sub bit line interconnected unit in the cell unit which includes the selected cross-point memory cell to the corresponding main bit line ~~and connect the word line to the second bias circuit~~, and a row decoder which decodes a row address signal and supplies the row address signal to the read word line driver.

Claim 8 (Currently Amended): The memory according to claim 7, wherein the third MOS transistor comprises an NMOS transistor, and an inverted signal of the signal supplied to the first switch ~~circuit~~ circuits is supplied to a gate of ~~the~~ each third MOS transistor for each cell unit.

Claim 9 (Currently Amended): The memory according to claim 7, wherein the third MOS transistor comprises a PMOS transistor, and the signal supplied to the first switch ~~circuit~~ circuits is supplied to a gate of ~~the~~ each third MOS transistor for each cell unit.

Claim 10 (Currently Amended): The memory according to claim 4, wherein the first bias circuit ~~stops~~ is configured to stop applying the bias voltage to the selected one main bit line on the basis of a column address select signal output from the CSL driver.

Claim 11 (Currently Amended): The memory according to claim 10, wherein the selected one main bit line is connected to the sense amplifier in response to the column address select signal, and a voltage substantially equal to the bias voltage output from the first bias circuit is applied from the sense amplifier to the selected one main bit line.

Claim 12 (Original): The memory according to claim 6, wherein the bias voltage output from the second bias circuit is substantially equal to the bias voltage output from the first bias circuit.

Claim 13 (Original): The memory according to claim 7, wherein the bias voltage output from the second bias circuit is substantially equal to the bias voltage output from the first bias circuit.

Claim 14 (Currently Amended): ~~The~~ A magnetic random access memory comprising:

a memory cell array of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line; and

word line potential setting means for, in read operation, setting, in a floating state, first word lines to which unselected cross-point memory cells connected to the sub bit line to which the selected cross-point memory cell is connected are connected, and setting word lines except the first word lines, which are connected to sub bit lines which do not include the selected cross-point memory cell to a potential substantially equal to a potential applied the main bit line.

Claim 15 (Currently Amended): The memory according to claim 14, wherein a potential of the word line connected to the selected cross-point memory cell is different from those of the word lines connected to unselected cross-point memory cells connected to the sub bit lines which do not include the selected cross-point memory cell.

Claim 16 (Original): The memory according to claim 14, further comprising bias means for holding the potential of the main bit line at a predetermined bias voltage.

Claim 17 (Original): The memory according to claim 16, wherein the bias means stops applying the bias voltage to the selected main bit line in response to a column address select signal which selects a column address of the memory cell array.

Claim 18 (Original): The memory according to claim 17, wherein the selected main bit line is connected to a sense amplifier in response to the column address select signal, and a voltage substantially equal to the bias voltage output from the bias means is applied from the sense amplifier to the selected main bit line.

Claim 19 (Currently Amended): A magnetic random access memory comprising:

a memory cell array of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line;

connection means for selectively connecting a word line ~~to select the memory cell~~ connected to a cross-point memory cell to be selected to one of first and second potential supply sources which are different from each other; and

control means for controlling the connection means to selectively connect the word line and to set ~~the~~ a further word line in an ~~electrical~~ electrically floating state[[.]], wherein

the control means comprises first and second row decoders and word line drivers to set a potential of the word line in the read mode, and

when the connection means is deactivated by the first and second row decoders and word line drivers, the further word line is set in the electrically floating state.

Claim 20 (Canceled).

Claim 21 (Currently Amended): The memory according to claim ~~20~~ 19, wherein the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of output signals from the first and second row decoders and word line drivers, each of the first and second selection circuits being constituted by an NMOS transistor, and ~~the MOS~~ each NMOS transistor is controlled by the output signals from the first and second row decoders and word line drivers.

Claim 22. (Original) The memory according to claim 21, wherein the signal supplied from the first row decoder and word line driver to the first selection circuit is independent for each sub bit line, and the signal supplied from the second row decoder and word line driver to the second selection circuit is independent for each word line.

Claim 23. (Currently amended) ~~The memory according to Claim 19~~ A magnetic random access memory comprising;

a memory cell array of hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line;

connection means for selectively connecting a word line connected to a cross-point memory cell to be selected to one of the first and second potential supply sources which are different from each other; and

control means for controlling the connection means to selectively connect the word line and to set a further word line in an electrically floating state, wherein

the control means comprises a row decoder and word line driver to set a potential of the word line in the read mode, and

when the connection means is deactivated by the row decoder and word line driver, the further word line is set in the electrically floating state, and

the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of an output signal from the row decoder and word line driver, each of the first and second selection circuits being constituted by an NMOS transistor, and each NMOS transistor is controlled by the output signal from the row decoder and word line driver.

Claim 24 (Canceled).

Claim 25 (Currently Amended): The memory according to claim ~~24~~ 23, wherein the signal supplied from the row decoder and word line driver to the first selection circuit is a signal obtained by logically inverting a select signal between the main bit line and the sub bit line, and the signal supplied from the row decoder and word line driver to the second selection circuit is independent for each word line.

Claim 26 (Currently Amended): A magnetic random access memory comprising:

a memory cell array of hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line;

connection means for selectively connecting a word line connected to a cross-point memory cell to be selected to one of first and second potential supply sources which are different from each other; and

control means for controlling the connection means to selectively connect the word line and to set a further word line in an electrically floating state, wherein

the control means comprises a row decoder and word line driver to set a potential of the word line in the read mode, and

when the connection means is deactivated by the row decoder and word line driver, the further word line is set in the electrically floating state, and

the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of an output signal from the row decoder and word line driver, the first selection circuit being constituted by a PMOS transistor, and the second selection circuit being constituted by an NMOS transistor, and ~~the MOS~~ each PMOS and NMOS transistor is controlled by the output signal from the row decoder and word line driver.

Claim 27 (Original): The memory according to claim 26, wherein the output signal supplied from the row decoder and word line driver to the first selection circuit is a select signal between the main bit line and the sub bit line, and the output signal supplied from the row decoder and word line driver to the second selection circuit is independent for each word line.

Claim 28 (Currently Amended): A method of reading data from a magnetic random access memory including a memory cell array of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line, comprising:

asserting a word line connected to a cross-point memory cell to be selected and setting first word lines ~~in a floating state, the word lines being~~ connected to unselected cross-point memory cells connected to the sub bit line to which the cross-point memory cell to be selected is connected in a floating state; and

setting second word lines ~~except the word lines, which are~~ connected to ~~the~~ sub bit lines which ~~do~~ are not ~~include~~ connected to the selected cross-point memory cell, to a potential substantially equal to the main bit line.

Claim 29 (Currently Amended): The method according to claim 28, further comprising

after setting the second word lines to the potential substantially equal to the main bit line,

connecting the sub bit line to which the selected cross-point memory cell is connected to the main bit line and selecting the main bit line and connecting the main bit line to a sense amplifier, and

causing the sense amplifier to detect and amplify stored data in the cross-point selected memory cell and read out the data.